Listing and/or Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Previously Amended) An apparatus for isolating a noise intolerant device from a source of noise, comprising:

a processor for producing clock and data signals and a control signal; and

a digital bus that couples said clock and data signals to a buffer,

where, in response to said control signal, said buffer selectively couples said clock and data signals to respective clock and data inputs of said noise intolerant device such that said noise intolerant device is operatively coupled to said processor via said digital bus only when said processor is communicating with said noise intolerant device.

2. (Previously Amended) The apparatus of claim 1, wherein said digital bus is an inter integrated circuit bus, and the apparatus further comprises an IIC bus expander for transferring said control signal to said buffer.

3. (Previously Amended) The apparatus of claim 1, wherein the digital bus comprises

an IIC bus having a clock signal path for transferring clock pulses from said processor to said clock inputs of said IIC bus expander and said buffer;

a data signal path for transferring data from said processor on said data signal path during each of said clock pulses on said clock signal path to said clock and data inputs of said IIC bus expander and said buffer; and

wherein, said output of said IIC bus expander, coupled to said buffer, selectively controls a clock output and a data output of said buffer for isolating said noise intolerant device from said IIC bus and said processor.

4. (Previously Amended) The apparatus of claim 3, wherein said noise intolerant device comprises:

a tuner, coupled to said clock and data outputs of said buffer device, having a phase-lock loop for generating frequency variable tones, and a down-converter coupled, to said phase-lock loop, for mixing one of a plurality of television signals with a one of said frequency variable tones to produce an IF television signal.

5. (Previously Amended) The apparatus of claim 4, wherein said buffer comprises:

a first OR gate and a second OR gate, each of said first and said second OR gates having a first input coupled to said output of said IIC bus expander;

a second input said first OR gate coupled to a clock signal path of said IIC bus, and a second input of said second OR gate coupled to a data signal path of said IIC bus; and

an output of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop, and an output of said second OR gate, being said data output of said buffer, coupled to said data input of said phase-lock loop.

6. (Currently Amended) A television receiver for receiving and processing television signals, apparatus comprising:

a controller assembly comprising an inter-integrated circuit bus having a clock signal path and a data signal path, a processor, coupled to said clock and data paths, an IIC bus expander coupled to said processor via said clock and data paths, and a buffer coupled to an output of said IIC bus expander;

a front-end assembly comprising a tuner having a down converter coupled to a phase-lock loop, said phase-lock loop coupled to an output of said buffer, at least one demodulator for demodulating said television signals, coupled to said down-converter, such that said phase-lock loop ~~noise intolerant device~~ is operatively coupled to said processor via said digital bus only when said processor is communicating with said phase-lock loop ~~noise intolerant device~~; and

at least one video and audio processor for processing said modulated television signals to produce audio and video signals.

7. (Previously Amended) The apparatus of claim 6, wherein said buffer comprises:

a first OR gate and a second OR gate, each of said first and said second OR gates having a first input coupled to said output of said IIC bus expander;

a second input of said first OR gate coupled to said clock signal path of said IIC bus, and a second input of said second OR gate coupled to said data signal path of said IIC bus; and

an output of said first OR gate, being said clock output of said buffer, coupled to said clock input of said phase-lock loop, and an output of said second OR gate, being said data output of said buffer, coupled to said data input of said phase-lock loop.

8. (Currently Amended) A method for isolating a phase-lock loop in a tuner of a television receiver, comprising the steps of:

sending a first command from a processor to a phase-lock loop via a digital bus to generate a frequency tone; and

sending a second command to a buffer to isolate said phase-lock loop from said processor, whereby said phase lock loop ~~noise intolerant device~~ is operatively coupled to said processor via said digital bus only when said processor is communicating with said phase lock loop ~~noise intolerant device~~.

9. (Previously Amended) The method of claim 8, wherein said first command sending step further comprises the steps of:

setting an inter-integrated circuit bus expander output to a LOW logical state, after receiving a request for a selected television signal from a user, in response to said first command by said processor; and

coupling said phase-lock loop to an IIC bus, for enabling said processor to communicate with said phase-lock loop to generate said frequency tone.

10. (Original) The method of claim 9 wherein said coupling step further comprises the step of:

enabling, in response bus expander output, a buffer to couple said phase-lock loop to said IIC bus.

11. (Original) The method of claim 9, wherein said second command sending step further comprises the step of:

setting an output of said buffer to a HIGH logical state after said phase-lock loop locks to said single frequency tone, in response to said second command from said processor.